aria CYBERSECURITY SOLUTIONS

DATASHEET

The Myricom ARC Series with DBL

Drive down system-level Tick-To-Trade latency and enable advanced financial trading capabilities with a tightly-integrated combination of FPGA firmware and software libraries

Features and Benefits

10GbE network adapters lead the industry in system-level Tick-To-Trade Latency

Tightly integrated FPGA firmware and server software combine to accelerate trading applications

Precise hardware timestamps on both ingress and egress packets

Support for Linux and Windows

ARIA Cybersecurity's Myricom® ARC Series of 10 gigabit network adapter integrated with DBL software surpasses all other full-featured adapters, with industry-leading latency plus advanced capabilities to accelerate your trading application, enable advanced trading capabilities and meet MiFID II reporting regulations.

Driving Latency Close to Zero

All ARC adapters minimize latency by exploiting the parallel processing capabilities of powerful FPGAs and integrated acceleration software libraries to:

- Move packets into the host computer with the lowest possible latency
- Send a subset of these packets directly to specific CPU cores, bypassing the kernel entirely
- Stage TCP market orders or quotes in advance to further reduce latency

System-level Tick-to-Trade Latency

DBL drives down Tick-To-Trade latency at multiple points in the trading process, allowing your application to deliver higher fill rates.

First, it minimizes Receive Latency by exploiting the parallel processing capabilities of powerful FPGAs to direct subsets of a multi-cast market feed to specified CPU cores, totally bypassing the OS kernel.

At initialization, your application uses our DBL software library for a quick and easy set-up of the selectors, targeting data from a specific address and port to an assigned ring.

(See Figure 1) Every packet does not need to move into the user space data rings, just the packets your application uses.

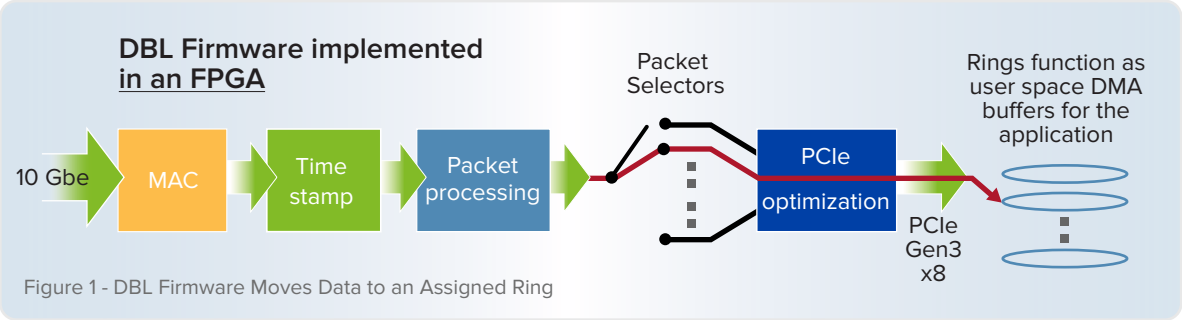


Figure 1 - DBL Firmware Moves Data to an Assigned Ring

Integrated DBL Software Accelerates the Application Layer

You can compress total Tick-To-Trade latency even further by accelerating your application with the tightly integrated DBL software (See Figure 2). Acceleration is delivered by Kernel Bypass Stacks, which move UDP packets directly to your application in user space. Doing that eliminates the cost of CPU context switches and also enables deployment of special-purpose network stacks in user space, which are faster than the general purpose stacks inside the kernel. The DBL software provides three interface options for implementing a faster network stack:

- Transparent Sockets allow your application to accelerate stack performance without code changes. Standard socket calls access the low latency DBL stack without recompiling.
- The DBL API accesses a set of Myricom-optimized sockets. It requires a software recompile, with renamed socket calls, but delivers even lower latency.
- Raw Mode allows customers to implement their own custom stacks with the Myricom ARC network adapters, using either raw sockets or a proprietary API.

In general, Raw Mode is useful for customers who have created their own UDP networking stacks to work with another vendor's products and are now migrating to the Myricom network adapters. Most longtime Myricom customers use the DBL API, gaining the advantages of a latency-optimized UDP stack function without investing time or money in additional software development.

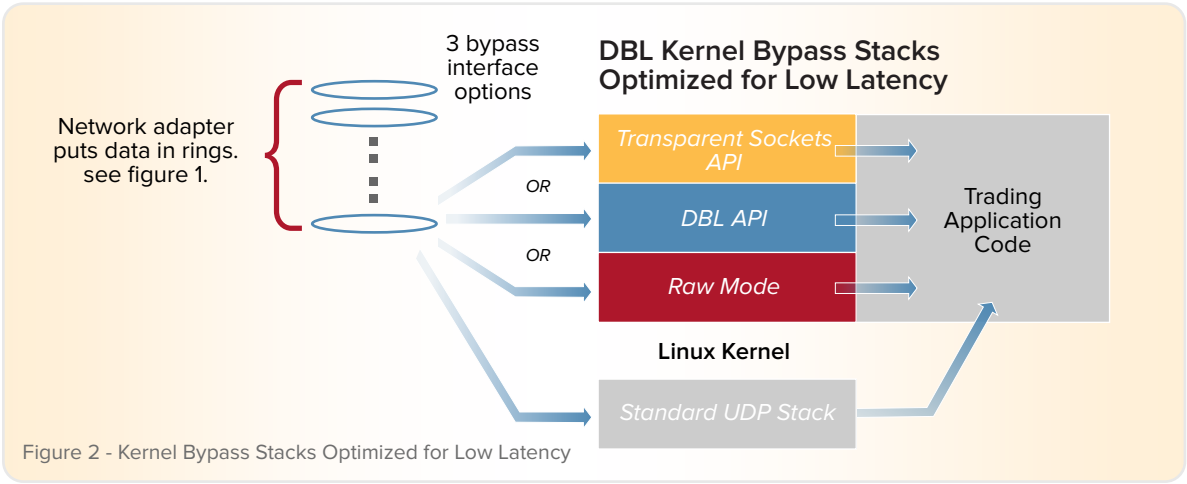


Figure 2 - Kernel Bypass Stacks Optimized for Low Latency

Reducing Send Latency

DBL software accelerates outbound order processing by pre-populating the TCP/IP stack in user space, then filling in just the variable information from the application before sending the BUY/SELL order packet to the adapter. The Send Latency is further minimized with extremely efficient PCIe to Ethernet conversion firmware.

Precise hardware Timestamps

With DBL firmware, the ARC adapters are able to track latency in real-time with less effort and more accuracy than expensive packet capture devices, using precise hardware timestamps on both ingress and egress packets. This unique capability allows your application to calculate and display latency in real-time without needing to tag TCP/IP orders with UDP sequence numbers, for simplified trading performance verification.

Precise timestamping also prepares trading systems for compliance with the detailed reporting defined in the MiFID II regulations. By implementing both Receive and Send timestamps in the Myricom ARC Series hardware, your trading application can meet the new transparency requirements while still executing with extreme low-latency.

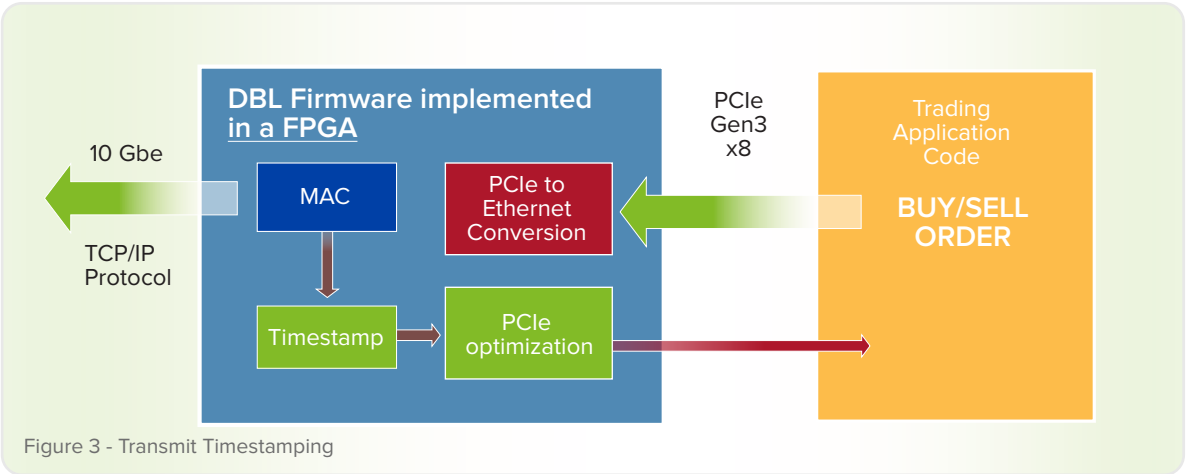
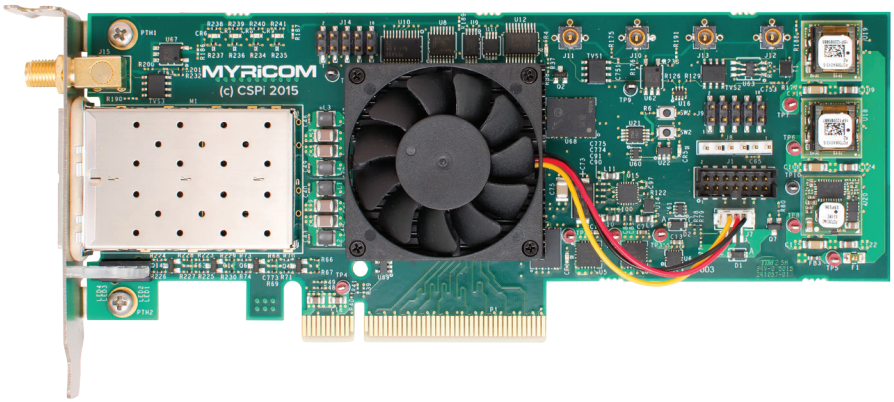


Figure 3 - Transmit Timestamping



E-Class

Features

- Industry's lowest latency
- Performance optimized FPGA
- Timing kit is standard

SPECIFICATIONS	Myricom ARC E
Dimensions	2.7" x 6.6" (dual)
Bus interface	PCI Express Gen 3, 8 lanes wide
Form factor	Dual port Low-profile PCI Express x8 add-in cards that ship with a standard height faceplate installed; and a low profile faceplate
Electrical power	18 W - dual port adapter
Cooling Requirements	It is recommended that adapters be installed into servers that provide some air flow over the PCIe slots. Use in an office or computer room environment.
Cooling Options	Active cooling
Operating Temperature	0-55 deg C (100 LFM min)
Storage Temperature	- 40 to 70 deg C
Storage Humidity	5% to 90% non-condensing
Processor	FPGA
Hardware Acceleration	N/A
Memory	No user programmable memory
Network Connectivity	2x10 GB Ethernet, SFP+
Software Support	Software available for Linux (CentOS, RHEL and Ubuntu) and Windows. Supports libpcap (Linux) and winpcap (Windows) libraries. Software provides support for RSS (receive side scaling), port merging of ethernet packets, pcap replay
SW Version supported	V5.0.7 – DBL No ethernet driver
Security	N/A

SPECIFICATIONS	Myricom ARC E
Throughput	2x10Gb/s
Timestamp (if applicable)	+/- 100 ns accuracy
Regulatory approvals, compliance	RoHS (Reduction of Hazardous Substances). EMI and EMC, Class A USA, Canada, and Europe.
WARRANTY AND COMPLIANCE	
Country of Origin	USA
Warranty	One year for hardware defects and 90 days for software defects. 90 days of "getting started" telephone and email support, as well as any software upgrades shipped within that window. Refer to the support datasheet for options extending the 90-day window
Ordering Details **(license can be purchased separately on already sold adapter).**	10G-PCIE3-8EL-2S+DBL Dual SFP+ board using K35 FPGA with DBL License. Low profile bracket pre-installed. SPT-10G-PCIE3-8EL-2S+DBL Annual support for Dual SFP+ board using K35 FPGA with DBL license. Includes software updates and email support.
Cables and transceivers	Contact your Account/Sales representative for more information on cables and transceivers that are compatible with this adapter.

Contact Us Today: ARIAsales@ariacybersecurity.com or 800.325.3110

ABOUT ARIA CYBERSECURITY SOLUTIONS

ARIA Cybersecurity Solutions recognizes that better, stronger, more effective cybersecurity starts with a smarter approach. Our solutions provide new ways to monitor all internal network traffic, while capturing and feeding the right data to existing security tools to improve threat detection and surgically disrupt intrusions. Customers in a range of industries rely on our solutions each and every day to accelerate incident response, automate breach detection, and protect their most critical assets and applications. With a proven track record supporting the Department of Defense and many intelligence agencies in their war on terror, and an award-winning portfolio of security solutions, ARIA Cybersecurity Solutions is committed to leading the way in cybersecurity success.

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