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NASDAQ: CSPI

Could you please explain the meanings of the DBL v4 hardware/software counters reported in the output of myri counters?

Model:

ARC Series D Adapters (10G-PCEI3-8D-2S).

Software:

DBL v4

Operating System:

Supports both Linux and Windows operating systems.

Information:

To obtain the values of the DBL v4 hardware and software counters since the driver was loaded (or since the counters were reset via **myri_counters –c),** use the tool **myri_counters.**

On Linux, this tool can be found in **/opt/dbl/bin/mri_counters.**

Example: `% /opt/dbl/bin/myri_counters`

On Windows, the **myri_counters.exe** executable can be found in the **[INSTALLDIR]/bin** directory.

By default, the **myri_counters** output is only displayed for port 0. Two-port adapters appear to myri_counters as different ports. If you have a two-port network adapter installed in the host, you will need to specify the command-line argument **–p <port_num>** to obtain the counters output for each port. For example:

```
% /opt/dbl/bin/myri_counters -p 0
% /opt/dbl/bin/myri_counters -p 1
```

**Note that the space between the "p" and the number is optional. Also, if a host contains two two-port adapters, you would use –p0 and –p1 for the ports of the first adapter and –p2 and –p3 for the ports of the second adapter. **

Usage Summary:

```
$ ./myri_counters -h
Usage: myri_counters [args]
-p - Port number [0] or Ethernet MAC
-c - clear the counters
-a - show counters for all endpoints. Default shows counters for only
endpoint 0.
-vv - show all counters
-q - quiet: show only nonzero counters
-i - show host interrupt counters
-x - expert: show all counters
-h - help
```

To clear/reset the counters requires root privileges. To clear the counter on a specific port of a network adapter use:

```
# /opt/dbl/bin/myri_counters -p <port_num> -c
```

All the counters are 64-bit counters. The majority of the counters are for **developer use only** and will not be defined below.

If you have additional questions on **Linux DBL**, please send the output of **$PERFIX/bin/phx_bug_report** to CSPI Technical Support (support@cspi.com).

If you have additional questions on **Windows DBL**, please send the output of the Windows **phx_bug_report.ps1** powershell script to CSPI Technical Support (support@cspi.com).

How to run the Windows phx_bug_report.ps1 powershell script:

Install phx-tools, DBL v4 or Sniffer v4

Open a Windows Powershell as Administrator (administrator privileges may be required to write to tools directory)

Change to tools directory

```
PS C:\> cd 'C:\Program Files\CSPi\phx-tools'
```

Run script, save result to file and send us the output. It typically takes about 20 seconds to complete.

```
PS C:\Program Files\CSPi\phx-tools> .\phx_bug_report.ps1 > output.txt
Gathering diagnostic information...Completed
```

**Windows: If you do not have DBL installed then you will receive the following error message from phx_bug_report.ps1:

```
C:\Program Files\CSPi\phx-tools\phx_bug_report.ps1 : ERROR: Could not find the DBL or
SNF executables
At line:1 char:1
+ .\phx_bug_report.ps1 > output.txt
+ ~~~~~~~~~~~~~~~~~~~~~~~~
    + CategoryInfo          : NotSpecified: (:) [Write-Error], WriteErrorException
    + FullyQualifiedErrorId :
Microsoft.PowerShell.Commands.WriteErrorException,phx_bug_report.ps1
```

Edit the **phx_bug_report.ps1** script to modify **the Driver Path** to point to the directory where the DBL or Sniffer (SNF) driver was installed. Typically, `C:\DBL_PHX-10G or C:\SNF_PHX-10G.`

The DBLv4 software has been installed on a 10G-PCIE-8D-2S network adapter. The 10G-PCIE-8D-2S adapter is a two port x8 Gen3 PCI-Express 10GbE adapter, and it is FPGA-based.

The **myri_counters** output is arranged in grouped blocks, based on which part of FPGA board the counter applies.

The 10G-PCIE-8D-2S adapter has 2 ports. Each port may have multiple dedicated endpoints, or the endpoints may be pooled and distributed by the kernel as a port requests them. Each port will have a MAC address associated with it.

The logical view of counters is also affected by the physical design of the FPGA internal IP. There are components of the FPGA design that are shared by all ports as well as parts that are duplicated and each port can only access its copy of the component.

There are 4 block types used to indicate the scope of a counter- **global, endpoint, port, and port-endpoint**. An excerpt from an example **myri_counters** output is included below:

```
$ sudo bin/myri_counters -v

Board 00:60:dd:43:cf:40 with 1 ports, 4 endpoints
global     :              PIO CP Read Dword:            6559
global     :              PIO CP Read Header:           5929
global     :              PIO CP Write Dword:        5003918487
global     :              PIO CP Write Header:       5003656639

endpoint  0 :            EP Packets Received:             0
endpoint  0 :              EP Bytes Received:             0
endpoint  0 :            EP TX PIO Packets:               0
endpoint  0 :              EP TX PIO Bytes:               0
endpoint  0 :            EP TX DMA Packets:               0
endpoint  0 :              EP TX DMA Bytes:               0
endpoint  0 :            EP Host RX Packets:              0
endpoint  0 : EP Host RX Packets with MAC Errors:         0
endpoint  0 :            EP TX Completions:               0
```

```
endpoint  0 :              EP Data Pages:              0
endpoint  0 :              EP Desc Pages:              0
endpoint  0 :      EP Data Consumer Position:              0
endpoint  0 :      EP Data Producer Position:              0
endpoint  0 :      EP Desc Consumer Position:              0
endpoint  0 :      EP Desc Producer Position:              0

port 0    :                Cycle Count:   0x00000009e7fc085a
port 0    :           Packets Received:              3000
port 0    :             Bytes Received:            180000
port 0    :        Pkts Received Filter:              3000
port 0    :        Bytes Received Filter:            180000
port 0    :          MAC Receive Errors:              0
port 0    :           Packets Filtered:              3000
port 0    :          Packets Unfiltered:              0
port 0    :           Packets Rx Filter:              3000
port 0    :        Packets Drop Incoming:              0
port 0    :      Intentional Discard Pkts:              0
port 0    :          Multicast Packets Rx:              0
port 0    :      Multicast Pkts Discarded:              0
port 0    :           Filter Add Slots:              4
port 0    :           Filter Used Slots:              0
port 0    :           Filter Free Slots:              511
port 0    :         RX Packet Count Limit:              8
port 0    :           RX Length Limit:   0x00000000ffffffff
port 0    :            RX Time Limit:              10
port 0    :            Packet Overflow:              0
port 0    :         Descriptor Overflow:              0
port 0    :      TX Pause MAC CTRL frames:              0
port 0    :      RX Pause MAC CTRL frames:              0

port 0 ep  0 :       EP Filter Packets Sent:              0
port 0 ep  0 :       EP Filter Bytes Sent:              0
```

In the above output, the **global** counters apply to FPGA as a whole. It does not matter which ports reads the register; it is the same register.

The **endpoint** counters are counts that apply to an endpoint. That endpoint may be permanently associated with a certain port, but in some cases it may be controlled by one port for a while and then a different port at a different time.

Port counters are counters that are associated with one physical port of the adapter. In all cases port counters are only dealing with the one specific port. When the actual counter is read in the FPGA it is a separate register for one port versus another, and the ports cannot access the registers in another port's address space.

The **per-port per-endpoint** registers exist in the port logic and are associated with moving packets to specific endpoints. The endpoints may be permanently associated with a given port, or not.

Revision	Date	Change
1	6/27/2016	Initial Draft
2	7/20/2016	Feedback